What is claimed is:

1. A method for compiling a user's design to allow greater access for reading and writing to memories and registers in the user's design, comprising;

identifying all of the memories and registers in the user's design;

synthesizing accessibility logic into the user's design, said accessibility logic creating access ports to the memories and registers.

2. The method of claim 1 further comprising the step of assigning a unique identifier to each of the memories and registers in the user's design.

3. The method of claim 2 wherein said accessibility logic comprises selecting logic, said selecting logic adapted to receive said unique identifier and select a particular one of the memories and registers in the user's design.

4. The method of claim 3 wherein said accessibility logic comprises logic to read from or write to said particular one of the memories and registers in the user's design.

5. The method of claim 4 wherein said accessibility logic comprises decode logic that receives commands from a host and controls execution of reading and writing data to the memories and registers in the user's design.

6. A hardware-assisted design verification system for verifying a target design, said verification system having a host workstation in communication with a hardware accelerator, the

target design comprising registers and memories, the host workstation loading data to or unloading data from the registers and memories, comprising:

protocol logic synthesized into the logic circuit, said protocol logic comprising:

an incoming packet register in communication with said host workstation;

an outgoing packet register in communication with said host workstation;

command decode logic, said command decode logic decoding a command in said incoming packet register to identify a particular operation, register or memory location in said target design;

write command execution logic to write data stored in said incoming packet register into said register or memory location in said target design for a write command decoded at said command decode logic;

read command execution logic to read data from said register or memory location in said target design and store said data in said outgoing packet register for a read command decoded at said command decode logic; and

interface logic interfacing said registers and memories in said target design.

7. The hardware-assisted design verification system of claim 6, wherein said protocol logic includes logic to determine whether data from said incoming packet register is new and control activation of command decoding and execution.

8. A method of synthesizing a packet-based protocol logic for providing access to registers and memories in a target design when performing functional verification using a hardware accelerator, comprising:

determining fixed sizes of a request packet, said request packet comprising tag, command, and data end fields;

counting how many of the registers are present in the target design;

counting how many of the memories are present in the target design;

determining a maximum identification field size of said request packet;

determining a maximum number of data bits of the registers in the target design;

determining a maximum number of data bits of the memories in the target design;

determining a maximum number of address bits of the memories in the target design; and

determining a maximum number of bits to send the register data, memory data, and memory address to the target design to determine data field size of said request packet.

9. The method of claim 8, further comprising the steps of:

creating an incoming packet register coupled to an input data buffer in the hardware accelerator;

creating an outgoing packet register coupled to an output data buffer in the hardware accelerator;

creating a command decode block to decode a command in said incoming packet register;

creating an execution logic to execute a command decoded at said decode block; and

creating interface logic to access the registers and memories in said target design.

10. The method of claim 9, further comprising the steps of:

creating a memory identification register to identify the memories in the target design;

creating a memory address register to provide a current memory address for access;

incrementing said current memory after a memory read command or a memory write command is executed;

creating a finite state machine to indicate that the packet-based protocol logic is in either non-memory mode, continuous memory write mode, or continuous memory read mode; and

creating a state transition control that selects said non-memory mode when said continuous memory operation ends, said state transition control further selecting said continuous memory write mode when said continuous memory write operation is initiated, said state transition control further selecting said continuous memory read mode when said continuous memory read operation is initiated.